

Fig. 1 is a schematic diagram of a multi-channel signal processing system. It shows a series of input channels (3) connected to a common output (4) via a series of intermediate stages (31). The output (4) is connected to a final output (41).

FIG 3

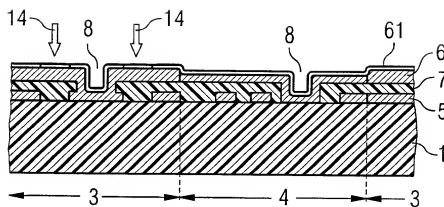


FIG 4

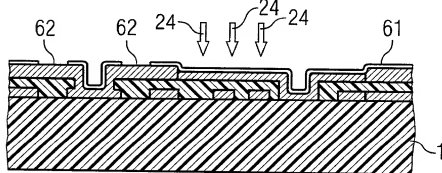


FIG 5

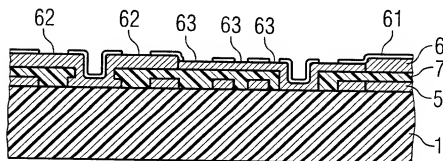


FIG 6

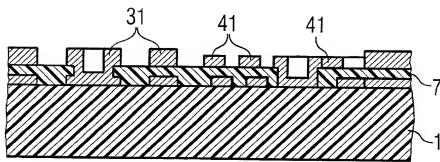


FIG 7

